Brushless DC Motor Drive with Power Factor Correction Controller Technique

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Abstract— In this paper we have proposed a power factor correction technique for permanent magnet brushless DC motor (PMBLDCM) drive. The proposed method improves the power quality of the system by reducing the harmonic contains in current source i.e. total harmonic distortion (THD) in the system. As THD gets reduced of the system, the power factor of the system is improved. To improve power factor of the system it is necessary to bring source current in phase with source voltage, which can be done by the boost converter. PMBLDC motors are best because of their high efficiency, silent operation, compact size, high reliability, and low maintenance requirements. The performance of the proposed system is simulated in MATLAB/Simulink environment.

Index Terms— Boost Converter, Diode Bridge Rectifier, Duty cycle, PMBLDC Motor, Power factor correction, Total harmonic distortion, Voltage Source Inverter.

1 INTRODUCTION

Efficiency and cost would be the major concerns in the development of low-power motor drives targeting household applications such as for example fans, water pumps, blowers, mixers, etc. The utilization of the brushless direct current (BLDC) motor in these applications is becoming very common due to options that come with high efficiency, high flux density per unit volume, low maintenance requirements, and low electromagnetic-interference problems. These BLDC motors are not limited to household applications, but they're ideal for other applications such as for example medical equipment, transportation, HVAC, motion control, and many industrial tools [5].

A BLDC motor has three phase windings on the stator and permanent magnets on the rotor. The BLDC motor can be referred to as an electronically commutated motor because an electronic commutation based on rotor position can be used rather than mechanical commutation which includes disadvantages like sparking and wear and tear of brushes and commutator assembly [5].

Power quality problems have become important issues to be looked at due to the recommended limits of harmonics in supply current by various international power quality standards. A BLDC motor when fed by way of a diode bridge rectifier (DBR) with a higher value of dc link capacitor draws peaky current which can cause a THD of supply current of the order of 60.44% and power factor as little as 0.85.Hence, a DBR followed by way of a power factor corrected (PFC) converter is utilized for improving the ability quality at ac mains. The decision of mode of operation of a PFC converter is just a critical issue since it directly affects the price and rating of the components used in the PFC converter. The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are the 2 modes of operation by which a PFC converter is designed to operate. In CCM, the present in the inductor or the voltage over the intermediate capacitor remains continuous, but it needs the sensing of two voltages (dc link voltage and supply voltage) and input side current for PFC operation, that is not cost-effective. On another hand, DCM requires someone voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains, but at the cost of higher stresses on the PFC converter switch hence, DCM is preferred for low-power applications [5].

The conventional PFC scheme of the BLDC motor drive utilizes a pulse width-modulated voltage source inverter (PWM-VSI) for speed control with a consistent dc link voltage. This offers higher switching losses in VSI while the switching losses increase as a square function of switching frequency. While the speed of the BLDC motor is directly proportional to the applied dc link voltage, hence, the speed control is accomplished by the variable dc link voltage of VSI. This enables the fundamental frequency switching of VSI (i.e., electronic commutation) and offers reduced switching losses. For further improvement in efficiency, bridgeless (BL) converters are employed which permit the elimination of DBR in the front end. A buck–boost converter configuration is most effective among various BL converter topologies for applications requiring a wide selection of dc link voltage control (i.e., bucking and boosting mode) [5].

2 BLDC MOTOR DRIVE

A PMBLDC motor accomplishes commutation electronically using rotor position feedback to determine when to switch the current. Feedback usually entails an attached Hall sensor or a rotary encoder .The stator windings work in conjunction with permanent magnets on the rotor to generate a nearly uniform flux density in the air gap. This permits the stator coils to be driven by a constant DC voltage (hence the name brushless DC), which simply switches from one stator coil to the next to generate an AC voltage waveform with a trapezoidal shape. A three-phase BLDC motor requires three Hall sensors to detect the rotor's position. Based on the physical position of the Hall sensors, there are two types of output: a 60° phase shift and a 120° phase shift. Combining these three Hall sensor signals can determine the exact commutation sequence.Advanced control algorithms and ultra-fast processors have made PMBL motors suitable for position control in machine tools, robotics and high precision servos, speed control and torque control in various industrial drives and process control application. A PFC converter forces the drive to draw sinusoidal supply current in phase with the supply voltage.It uses a DC-DC converter topology, boost converter, to obtain improved PF with improved performance, such as reduction of AC mains current harmonics, reduction of acoustic noise minimum number of components, maximum efficiency, etc. [3], [4].

3 CONVENTIONAL TOPOLOGY BLDC DRIVE

The low-power adjustable speed drives are powered from single-phase AC mains through a diode bridge rectifier (DBR) with smoothening DC capacitor and voltage source inverter (VSI).

Fig.1 shows the conventional topology.It contains DBR-VSI fed BLDC motor drive. Fig.2 shows the conventional topology simulated in MATLAB/Simulink. Fig.3 shows the AC mains current waveform and THD of conventional system. Because of the fact that, the DBR does not draw any current from the AC network when the AC voltage is less than the DC link voltage, as the diodes are reverse biased during that period however, it draws a peaky current when the AC voltage is higher than the DC link voltage.This results in a pulsed input current waveform featuring a peak value higher than thepeak of the fundamental input current thereby 60.38% total harmonic distortion (THD) in the input current [1], [2]. The power factor obtained is 0.85.

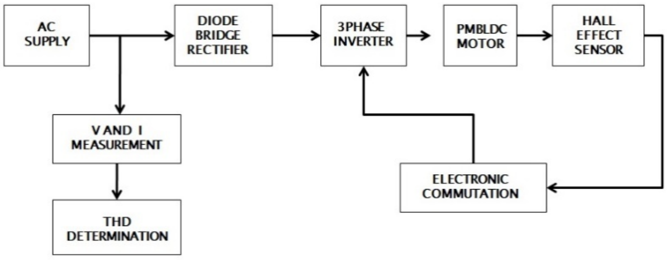

Fig.1. Block diagram of conventional topology BLDC drive

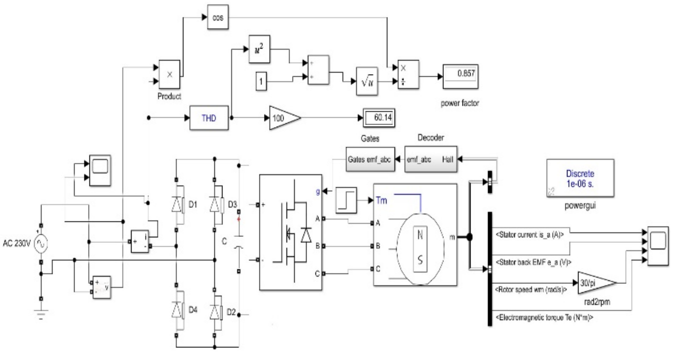

Fig.2.Conventional topology BLDC drive simulated in MATLAB/Simulink

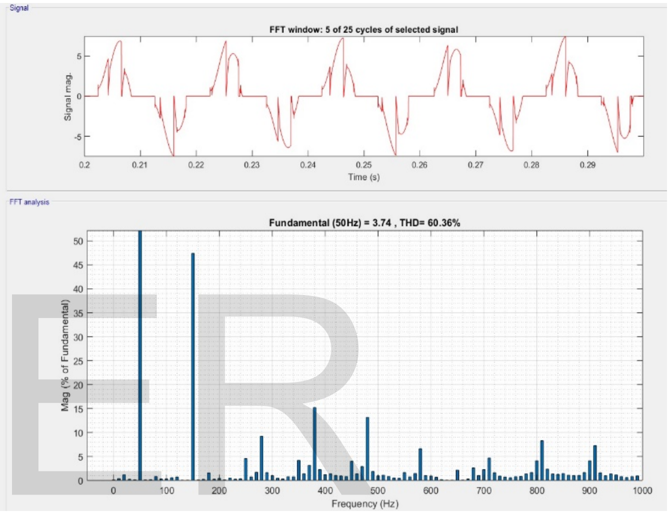

Fig.3. AC mains current waveform and its THD in conventional topology obtained from FFT Analysis in MATLAB/Simulink

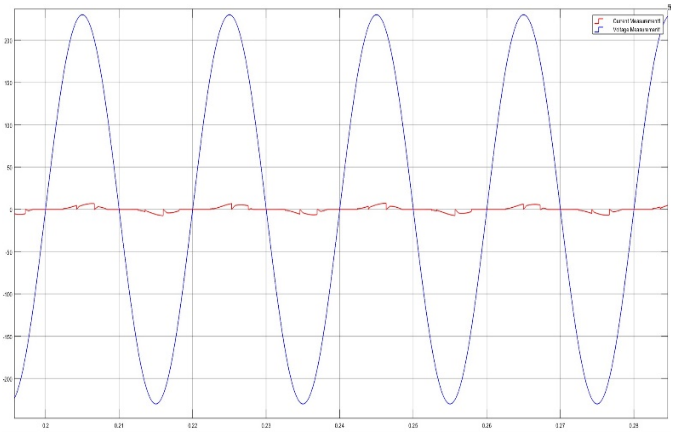

Fig.4. AC mains source current and source voltage waveform in conventional topology obtained from MATLAB/Simulink

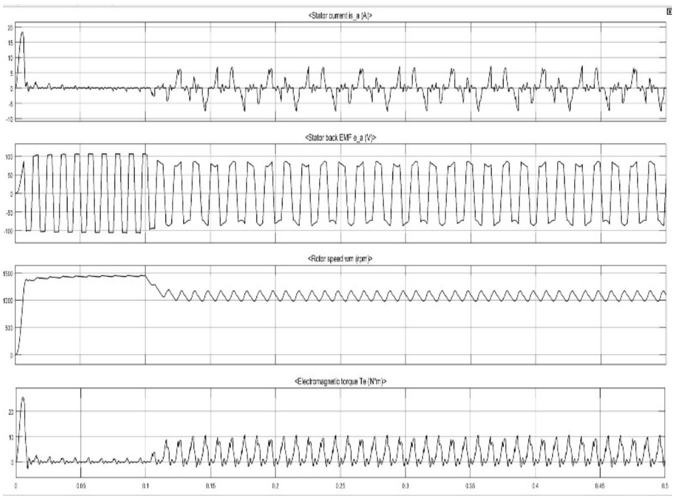

Fig.5. Waveforms of stator current, stator back EMF, rotor speed and torque obtained in MATLAB/Simulink

4POWER FACTOR CALCULATION

It is a measurement of the degree of the utilization of the power from grid. Mathematically it is the proportion of the real power to the apparent power and is in the range of 0 to 1.

$$Power\ factor = \frac{Real\ Power}{Apparent\ Power} \qquad (1)$$

Real power is in watts and is the power necessary for real work done. Apparent power is in volt-amp and is the vector summation of active and reactive power.
For pure sinusoidal voltage and current waveforms

$$Power\ factor = cos\emptyset \qquad (2)$$

Where “Cosø “is the displacement factor of the voltage and current. In general PFC tends to the compensation of the displacement factor. But for non-linear load i.e; for sinusoidal line voltage and non-sinusoidal line current waveform the PF can be expressed as;

$$\begin{aligned} pf &= \frac{V_{rms} \times I_{1rms}}{V_{rms} \times I_{rms}} cos\emptyset \\ &= \frac{I_{1rms}}{I_{rms}}\ cos\emptyset \\ &= Kp\ cos\emptyset \qquad (3) \end{aligned}$$

$$Kp = \frac{I_{1rms}}{I_{rms}} = \frac{I_{1rms}}{\sqrt{I_{irms}^2 + I_{2rms}^2 + \cdots + I_{nrms}^2}} \qquad (4)$$

Hence in practical PF is proportional to both harmonic content & displacement factor. Where n is the nth order of the harmonic current.
The total harmonic distortion factor is defined as;

$$THD_i = \frac{\sqrt{I_{2rms}^2 + I_{3rms}^2 + \cdots + I_{nrms}^2}}{I_{1rms}} = \frac{\sqrt{\sum_{n=2}^{\infty} I_{nrms}^2}}{I_{1rms}} \qquad (5)$$

$$Kp = \frac{1}{\sqrt{1 + THD_i^2}} \qquad (6)$$

Hence in simple, the power factor correction is referred as the minimization of the line current harmonic. The main objective of the the paper is power factor improvement i.e. maintaining a least phase angle between the input voltage and current with improved THD level i.e. keeping the harmonic content to a minimum level.

5 DC DC BOOST CONVERTER

5.1 Working of Boost Converter

The circuit diagram of a step up operation of DC-DC converter (Boost Converter) is shown in Fig.6. When the switch is closed for time duration, the inductor current rises and the energy is stored in the inductor. If the switch is opened for time duration, the energy stored in the inductor is transferred to the load via the diode and the inductor current falls. The waveform of the inductor current is shown in Fig.7.

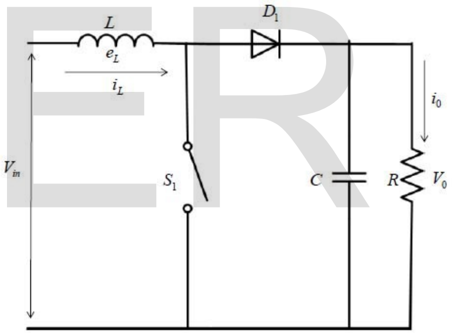

Fig.6. DC-DC Converter (Boost converter).

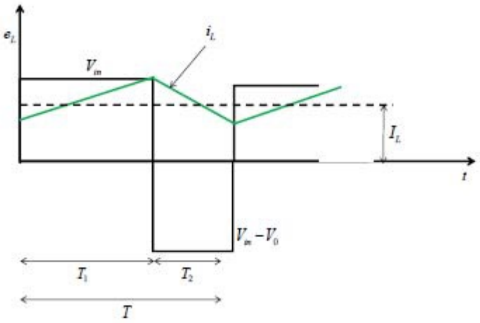

Fig.7. Inductor current waveform

5.2 Design of Boost Converter

Vout=300V, Iout=3A
Vinput(max)=230V, Vinput(min)=100V
Fs= 5khz.

$$D = 1 - \frac{Vin(\min) \times \eta}{Vout} \tag{7}$$

Assumed efficiency of converter as 80%, we have D=0.76

$$L = \frac{Vin \times (Vout - Vin)}{\Delta IL \times fs \times Vout} \tag{8}$$

$$\Delta IL = 0.4 \times Iout(\max) \times \frac{Vout}{Vin} \tag{9}$$

From equation 8 and 9 we have $\Delta IL=1.57A$ and $L=6.85mH$

$$Cout(\min) = \frac{Iout(\max) \times D}{fs \times \Delta Vout} \tag{10}$$

So, Cout (min) =219uF

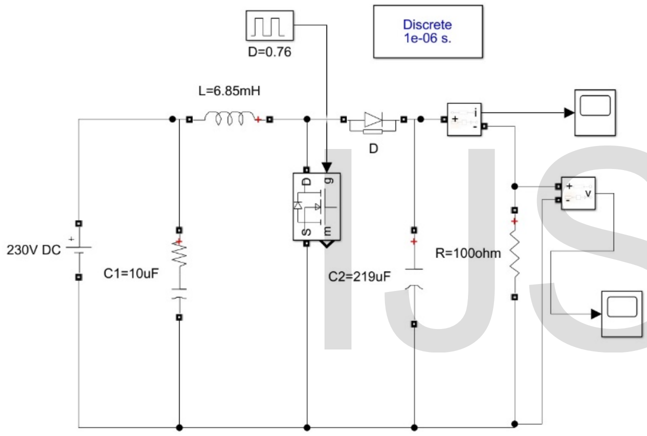

Fig.8. DC DC Boost Converter circuit simulated in MATLAB/Simulink

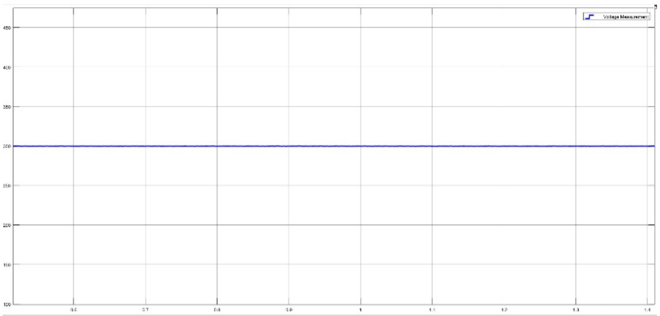

Fig.9. Output voltage 300V obtained from simulation of Boost converter circuit in MATLAB/Simulink

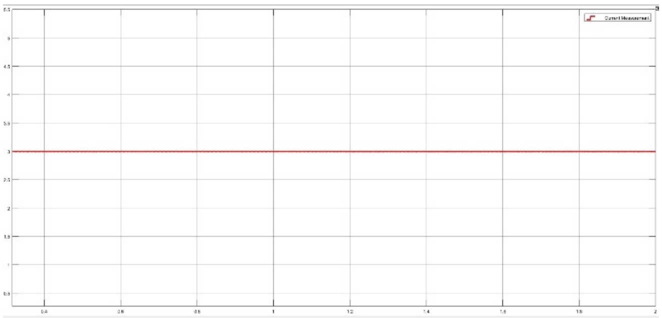

Fig.10. Output current 3A obtained from simulation of Boost converter circuit in MATLAB/Simulink

6 PROPOSED TOPOLOGY BLDC DRIVE

In the proposed PFC topology a boost converter is used to boost the input voltage which is fed to a voltage source inverter (VSI), the PMBLDC motor is given its supply from this VSI.

The main components of proposed PMBLDC system are DC DC boost converter, DBR, VSI, Hall Effect sensors, BLDC motor, PFC technique [12].

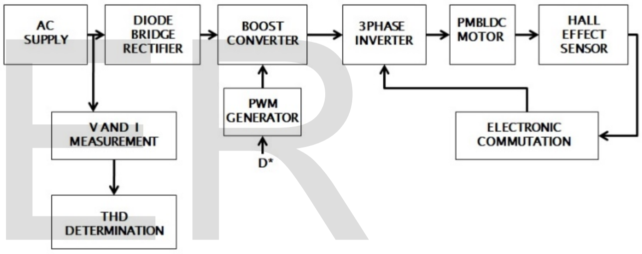

Fig.11. Block diagram of proposed topology BLDC drive

7 RESULTS

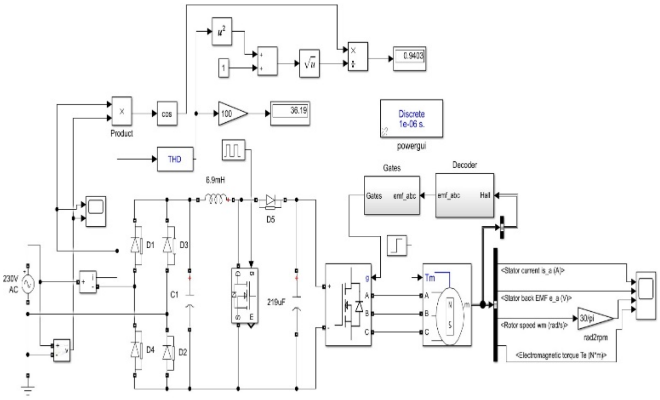

Fig.12. Proposed topology simulated in MATLAB/Simulink

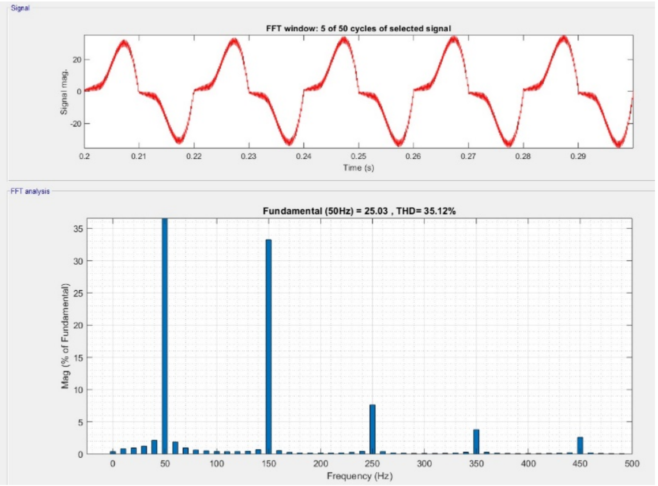

Fig.13. AC mains current waveform and its THD in proposed topology obtained from FFT Analysis in MATLAB/Simulink

The performance of converter fed BLDC motor drive is simulated in MATLAB/Simulink environment Fig.12. VSI fed PMBLDC motor is started at no load for stabilizing of DC link voltage. The power quality is monitored through FFT analysis of source current under steady state condition. Boost PFC converter shows very good response with input AC mains current THD of 35.46%, along with Pf of 0.9425.

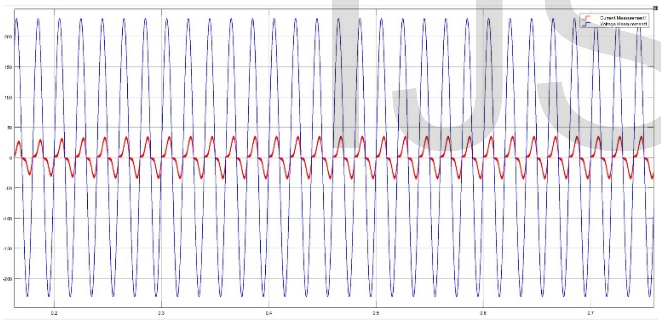

Fig.14. AC mains source current and source voltage waveform in proposed topology obtained from MATLAB/Simulink

Above Fig.14 shows source voltage, source current and below Fig.15 shows motor speed, stator current, stator voltage and torque for proposed VSI based topology fed PMBLDCM drives in steady state condition. The source voltage and current are in phase with each other as shown in Fig 13. The performance of the PMBLDCM drive is improved with boost PFC topology in terms of low torque ripples, smooth speed variation and improved power factor at AC mains.

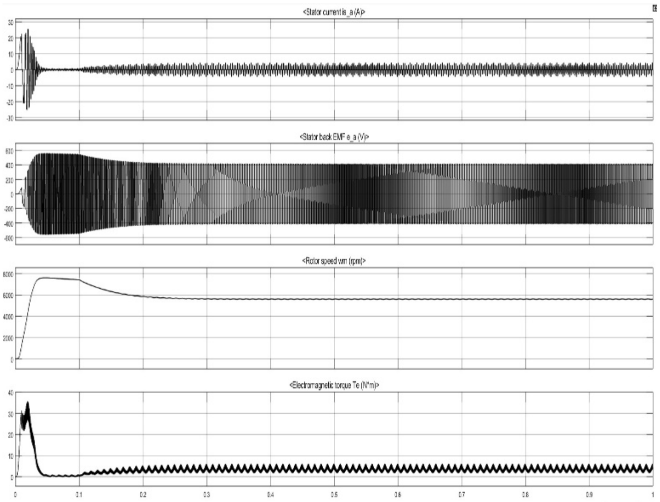

Fig.15. Waveforms of stator current, stator back emf, rotor speed and torque obtained in MATLAB/Simulink.

Table.1 Power factor and THD in source current with different values of Duty cycle obtained from MATLAB/Simulink.

Sr.no	Duty cycle %	THD %	Pf
1	10	74.33	0.8026
2	15	71.29	0.8143
3	20	68.85	0.8237
4	25	66.27	0.8336
5	30	64.08	0.8419
6	35	61.95	0.8501
7	40	59.85	0.8581
8	45	57.88	0.8655
9	50	55.64	0.8738
10	55	53.32	0.8824
11	60	50.83	0.8914
12	65	48.02	0.9015
13	70	44.81	0.9126
14	75	40.96	0.9254
15	80	36.45	0.9395
16	85	35.46	0.9425
17	90	47.55	0.9031

8 CONCLUSION

In this paper we have designed a model of PMBLDC motordrives for power quality improvement with power factor correction (PFC) topology. With conventional topology the THD in the source current was 60.38% and Power factor was 0.85 and after proposed topology it is reduced up to 35.46% and Power factor is improved to 0.94. The optimum value of duty cycle for Boost converter to achieve Power factor of 0.94 was 85%. By reducing THD in the source current Power factor of the system is improved. For that a Boost converter for VSI fed BLDC motor drive has been designed for achieving improvement in Power factor at AC mains for the development of low cost PFC motor for numerous low power equipment's such fans, blowers, water pumps etc. The proposed drive system is recommended for low power BLDC motor drives.

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